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| 10/681,446 | 10/06/2003 | Grant H. Kobayashi | P15733 | 1194 |

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| EXAMINER | |
|---|---|
| LEE, CHRISTOPHER E | |
| **ART UNIT** | **PAPER NUMBER** |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/681,446 | KOBAYASHI ET AL. | |
| | Examiner | Art Unit | |
| | Christopher E. Lee | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-25 and 32-53* is/are allowed.

6)☒ Claim(s) *26-31,54-59 and 61* is/are rejected.

7)☒ Claim(s) *60* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Receipt Acknowledgement*

1. Receipt is acknowledged of the Amendment filed on 28th of September 2007. Claims 31, 40, 45, 48-51, and 54-59 have been amended; no claim has been canceled; and no claim has been newly added since the RCE Non-Final Office Action was mailed on 29th of March 2007. Currently, claims 1-61 are pending in this Application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 54-59 and 61 are rejected under 35 U.S.C. 102(a) as being anticipated by Zimmer et al. [US 2003/0093579 A1; hereinafter Zimmer].

*Referring to claim 54,* Zimmer discloses a system comprising (i.e., a SYSTEM for concurrent handler execution in a SMI-based framework to service an SMI; See Abstract) comprising:

- a memory (i.e., SMM-Only Memory 26 of Fig. 1) to hold system management interrupt (SMI) code (i.e., add-on SMM event handler portion 38 of Fig. 1) beginning at a first memory address (i.e., a memory location for said add-on SMM event handler portion 38 within SMM-Only Memory 26 in Fig. 1; See paragraph [0037]);
- a first processor (i.e., processor CPU1 50 of Fig. 1) coupled to the memory (i.e., said SMM-Only Memory) to execute the SMI code beginning at the first memory address to

handle an SMI for the first processor in response to receiving the SMI (See paragraph [0042]); and

- a second processor (i.e., processor CPU2 51 of Fig. 1) coupled to the memory (i.e., said SMM-only Memory) to execute the SMI code beginning at the first memory address to handle the SMI for the second processor (See paragraphs [0053]-[0055]) in response to the SMI being software generated (i.e., in response to inter-processor interrupt IPI; See paragraph [0039]).

*Referring to claim 55,* Zimmer teaches

- the first processor (i.e., processor CPU1 50 of Fig. 1) is associated with a first system management base (SMBase) address (i.e., CPU default SMRAM address 0x3000-segment, offset 0x8000; See paragraph [0064], lines 1-4).

*Referring to claim 56,* Zimmer teaches

- the second processor (i.e., processor CPU2 51 of Fig. 1) is associated with a second SMBase address (i.e., platform address; See paragraph [0065], lines 1-5).

*Referring to claim 57,* Zimmer teaches

- the first memory address (i.e., a memory location for said add-on SMM event handler portion 38 within SMM-Only Memory 26 in Fig. 1) has an offset from the first SMBase address (See paragraphs [0064]).

*Referring to claim 58,* Zimmer teaches

- a target SMBase (e.g., platform address) referenced by the SMI code, by default, is the first SMBase address (i.e., default CPU address (0x38000p) to said platform address; See paragraph [0065]).

*Referring to claim 59,* Zimmer teaches

- the target SMBase is changed (i.e., relocated) to the second SMBase address before the second processor executes the SMI code (See paragraphs [0064]).

*Referring to claim 61,* Zimmer teaches

- the first and second processors (i.e., processors CPU1 50 and CPU2 51 in Fig. 1) are physical processors (See paragraph [0029]).

***Withdrawal the indicated Allowability***

4. The indicated allowability of claims 26-31 are withdrawn in view of the newly reconsidered reference to Zimmer [US 2003/0093579 A1] of the record. Rejections based on the newly reconsidered reference follow.

5. Claims 26-31 are rejected under 35 U.S.C. 102(a) as being anticipated by Zimmer [US 2003/0093579 A1].

*Referring to claim 26,* Zimmer discloses a method (i.e., a method for concurrent handler execution in a SMI-based framework to service an SMI; See Abstract) comprising:

- receiving a system management interrupt (SMI; See paragraph [0039]);
- executing a SMI handler (i.e., add-on SMM event handler portion 38 of Fig. 1) on a first processor (i.e., processor CPU1 50 of Fig. 1) to handle the SMI for the first processor (See paragraph [0042]); and

- executing the SMI handler (i.e., said add-on SMM event handler portion) on a second processor (i.e., processor CPU2 51 of Fig. 1) to handle the SMI for the second processor (See paragraphs [0053]-[0055]).

*Referring to claim 27,* Zimmer teaches

- the SMI is a software generated SMI (i.e., being generated in response to inter-processor interrupt IPI; See paragraph [0039]).

*Referring to claim 28,* Zimmer teaches

- the first processor (i.e., processor CPU1 50 of Fig. 1) executes the SMI handler (i.e., add-on SMM event handler portion 38 of Fig. 1) to handle the SMI for the first and the second processor (i.e., said add-on SMM event handler portion including Handlers 2-N for said CPU1 50 and CPU2 51 in Fig. 1; See paragraphs [0053]-[0055]).

*Referring to claim 29,* Zimmer teaches

- the SMI handler (i.e., add-on SMM event handler portion 38 of Fig. 1) is located at a first memory address (i.e., a memory location for said add-on SMM event handler portion 38 within SMM-Only Memory 26 in Fig. 1; See paragraph [0037]).

*Referring to claim 30,* Zimmer teaches

- the first memory address (i.e., a memory location for said add-on SMM event handler portion 38 within SMM-Only Memory 26 in Fig. 1) is a default offset from a first system management base (SMBase) address (i.e., CPU default SMRAM address 0x3000-

segment, offset 0x8000) associated with the first processor (i.e., processor CPU1 50 of Fig. 1; See paragraphs [0063]-[0064]).

*Referring to claim 31,* Zimmer teaches

- changing a target SMBase of the SMI handler (i.e., add-on SMM event handler portion 38 of Fig. 1) from the first SMBase address (i.e., CPU default SMRAM address 0x3000-segment, offset 0x8000) to a second SMBase address associated with the second processor (i.e., platform address; See paragraph [0065], lines 1-5); and
- executing the SMI handler (i.e., said add-on SMM event handler portion) using the second SMBase address as the target SMBase (See paragraph [0065], lines 8-11).

***Allowable Subject Matter***

6. Claims 1-25 and 32-53 are allowed.

7. Claim 60 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 1, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that receiving a first system management interrupt (SMI) with a first and a second processor; handling the first SMI with the second processor; generating a wake-up signal with the first processor after receiving the first SMI; awakening the second processor, based on the wake-up signal from the first processor; and handling the first SMI with the second processor.

The claims 2-11 are dependent claims of the claim 1.

With respect to claim 12, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that executing code at a first memory location with a first processor in response to the first SMI; and executing the code from the first memory location with the second processor, in response to the first SMI after awakening the second processor.

The claims 13-25 are dependent claims of the claim 12.

With respect to claim 32, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that checking if the SMI is a software generated SMI; and executing the SMI code to handle the SMI for a second processor, if the SMI is software generated.

The claims 33-39 are dependent claims of the claim 32.

With respect to claim 40, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that the first logical processor generates a wake-up signal after receiving the first SMI, wherein the wake-up signal references a first memory address of a default SMI handler; and the second logical processor to handle the first SMI after the wake-up signal is received from the first logical processor.

The claims 41-44 are dependent claims of the claim 40.

With respect to claim 45, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that the first processor is to generate a wake-up signal after receiving the first SMI; and the second logical processor to handle the first SMI after receiving the wake-up signal, wherein the second processor is to execute the code beginning at the first memory address to handle the first SMI.

The claims 46-53 are dependent claims of the claim 45.

With respect to claim 60, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that the first and second processors are logical processors.

***Response to Arguments***

9. Applicant's arguments with respect to claims 26-31, 54-59, and 61 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Zimmer [US 6,848,046 B2] discloses SMM loader and execution mechanism for component software for multiple architectures.

Cottrell [US 2004/0034854 A1] discloses method for meeting SMI duration limits by time slicing SMI handlers.

Harrington et al. [US 7,146,515 B2] disclose system and method for selectively executing a reboot request after a reset to power on state for a particular partition in a logically partitioned system.

Garvey [US 6,374,338 B1] discloses method for performing configuration tasks prior to and including memory configuration within a processor-based system.

Lee et al. [US 6,842,857 B2] disclose method and apparatus to concurrently boot multiple processors in a non-uniform-memory-access machine.

Hill et al. [US 6,925,556 B2] disclose method and system to determine the bootstrap processor from a plurality of operable processors.

O'Shea et al. [US 6,611,911 B1] disclose bootstrap processor election mechanism on multiple cluster bus system.

Tetrick et al. [US 5,768,585 A] disclose system and method for synchronizing multiple processors during power-on self testing.

Collins [US 6,158,000 A] discloses shared memory initialization method for system having multiple processor capability.

Dove et al. [US 5,938,765 A] disclose system and method for initializing a multimode multiprocessor computer system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on Monday through Friday, 6:00am - 2:30pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher E. Lee
Primary Patent Examiner
Art Unit 3992

/CEL./